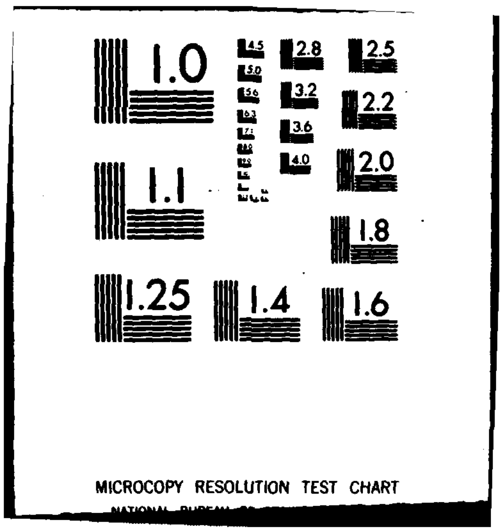
AD-A093 718 NAVAL SURFACE WEAPONS CENTER DAHLGREN VA F/G 19/5
VERIFICATION AND EVALUATION SYSTEM FOR TRIDENT (VEST): SUMMARY --ETC(U)
MAY 80 W L MCCOY
UNCLASSIFIED NSWC/TR-80-122 NL

1 of 1

END
DATE FILMED
2-81
DTIC


1.0
4.5
5.0
5.6
6.3
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.1
1.8
1.25
1.4
1.6
MICROCOPY RESOLUTION TEST CHART

AD A093718

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NSWC/TR-80-122	2. GOVT ACCESSION NO. AD-A093	3. RECIPIENT'S CATALOG NUMBER 728
4. TITLE (and Subtitle) VERIFICATION AND EVALUATION SYSTEM FOR TRIDENT (VEST): SUMMARY TO MANAGEMENT.		5. TYPE OF REPORT & PERIOD COVERED Final Rept.
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) W. L. McCoy		8. CONTRACT OR GRANT NUMBER(s) OMN 28
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Surface Weapons Center Code K54 Dahlgren, Virginia 22448		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Strategic Systems Project Office Department of the Navy Washington, DC 20376		12. REPORT DATE May 1980
		13. NUMBER OF PAGES 16
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

TRIDENT Fire Control System
VEST

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Verification and Evaluation System for TRIDENT (VEST): Summary to Management has been prepared by the Naval Surface Weapons Center (NSWC) for distribution to those persons and activities engaged in software development/production and life-cycle maintenance for the TRIDENT Digital Control Computer (DCC).

The VEST is an advanced hardware and software tool which has been developed to aid in software verification and validation (V&V), evaluate total system

20. ABSTRACT (Cont'd)

performance, aid with software debug, and assist with predicting the impact of proposed system modifications. The system produces automated reports and graphs, several types of which are appropriate for viewing by management.

This document is intended to communicate to the TRIDENT community the overall capabilities of the system, and its potential worth in life cycle support of the present system and constructing models for future systems.

FOREWORD

The Verification and Evaluation System for TRIDENT (VEST): Summary to Management is intended for program managers and lead engineers. It summarizes those aspects of VEST which are believed to be of interest to those directing and planning TRIDENT Fire Control Projects.

In terms of content, this summary is of a higher level than the VEST Concepts and Capabilities Document and the VEST Development Specification, which may be referred to for more specific technical details about the capabilities of the system.

For further information on VEST or to direct comments concerning this publication, contact the Naval Surface Weapons Center (NSWC), FBM Geoballistics Division, Code K54, Dahlgren, Virginia 22448.

Released by:

R. T. RYLAND, JR., Head
Strategic Systems Department

Accession For		
NTIS GRA&I	X	
DTIC TAB	☐	
Unannounced	☐	
Justification		
By		
Distribution/		
Availability Codes		
Dist	Avail and/or Special	
A		

CONTENTS

ILLUSTRATIONS

BACKGROUND

Throughout the life cycle of real-time, embedded computer systems, numerous situations arise which require access to detailed system performance data. The evolutionary nature of embedded computer systems often requires them to be modified as well as maintained. Given this, coupled with the additional problem of verifying and validating delivered software and changes thereto, and the need often to recreate and solve obscure problems reported from the field, there is considerable justification for a system like the Verification and Evaluation System for TRIDENT (VEST).

In 1973 when design of the TRIDENT Fire Control System was begun, it was clear that the inaccessibility of certain performance data had compounded, if not directly caused, many problems with earlier systems. Real-time software appeared to be a recurring problem area in which there rarely seemed to be a comfortable amount of performance data. Such software difficulties were most always related to hardware operating characteristics. Often the interrelationships could be discovered only after problem identification through painstaking investigation, sometimes requiring design of unique measurement configurations. To attack these problems, the decision was made to design a passive Performance Evaluation Interface (PEI) into the TRIDENT Digital Control Computer (DCC). This interface was to provide data quantities including Program Status Word (PSW), instruction being executed, memory location being referenced and contents thereof, and results of instruction execution, to an external port at minor cycle clock speeds. This interface was later used by the VEST measurement system.

GENERAL APPROACH TO THE PROBLEM

Software is usually delivered after being tested by a relatively small set of test cases, and this leaves a host of unknowns.

First, there is the question of test coverage. The criteria for adequacy of software testing is not established, but management could gain some confidence if

it knew that at least a minimal test set had been used, say, to cover all branches of the program. Such branch tracing is one of the possibilities with VEST.

How well does the system perform? The answer to this question is usually not immediately apparent because the true worst case has probably not been well defined for every time frame. The difficulty in setting up realistic loads and being able to closely monitor some of the subtle interactions of the hardware and software makes it essential that better measurements be taken than have usually been done in the past. One typical performance measurement is the closeness to time margins, i.e., the performance in meeting response time requirements and deadlines. These and other quantitative measurements such as idle time and memory activity can lead to an answer to the question of reserve capacity.

The lack of detailed knowledge about the actual inner workings of the software tends to hide trouble areas and, first of all, make it difficult to identify candidates for improvement. Then, if any modifications are proposed, there is the problem of determining the impact of modification.

The above uncertainties result in a "leave it alone" syndrome, and/or modifications by "trial and error," and, of course, the receipt of many Field Trouble Reports (FTRs) soon after the software reaches the operating forces. A better approach is, after the system is developed, to measure and analyze it, and document the results. This should verify test coverage, determine closeness to time margins, identify anomalies and bottlenecks, quantify reserve capacity, and identify improvements. For future systems or modifications to the current, the above results should act as a guide and also be used to construct models to assist future design efforts. (See Figure 1.)

THE VEST SOLUTION

This system permits a complete analysis of the system behavior under real-time operational scenarios. This is expected to result in the following benefits:

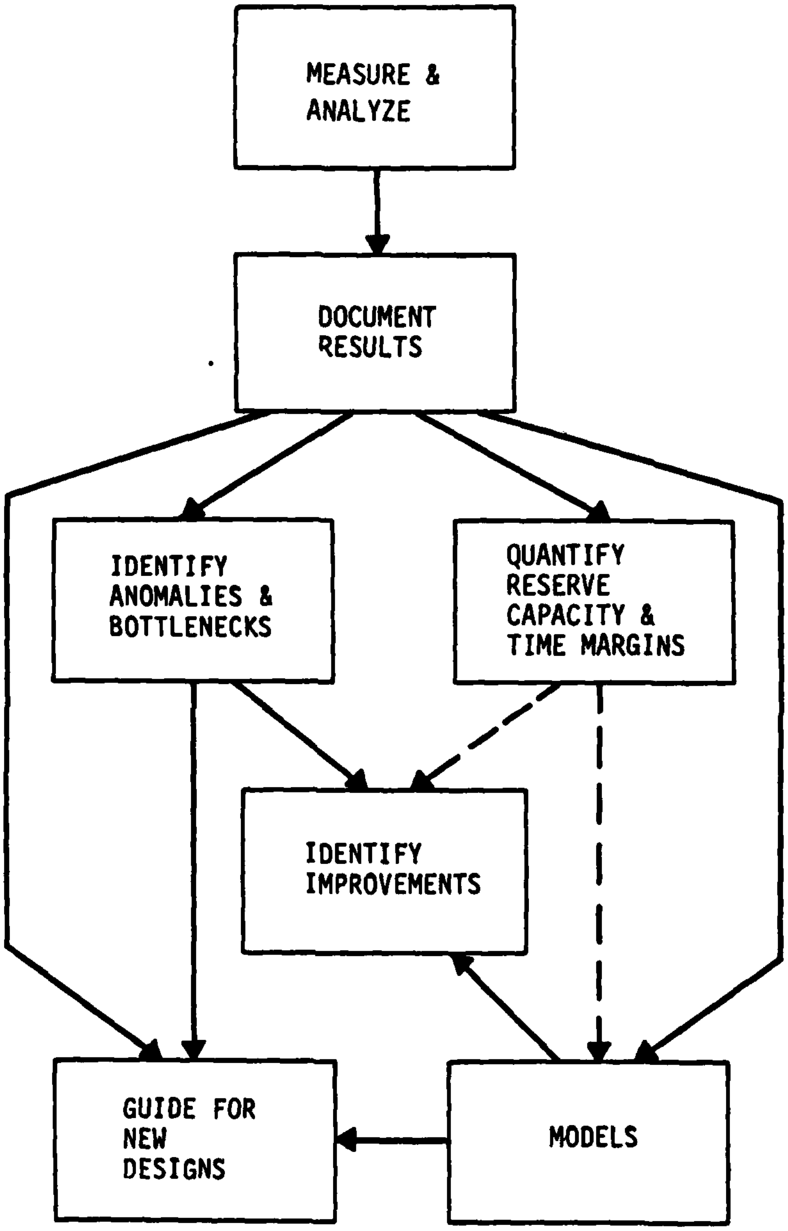


Figure 1. The VEST Approach

1. Enhanced software verification and validation (V&V) through verified program coverage, path coverage, correct program sequencing, and coordinated software deadlines.

2. Identification of reserved capacity and growth potential of the system, and conversly potential bottlenecks, by characterization of utilization levels, closeness to time margins, and system device idle time.

3. Reduced software costs for investigating sporadic malfunctions by providing a trace of hardware and software activity immediately preceding the failure which will lead to quicker problem resolutions.

4. Quantification of system performance parameters needed to drive models which in turn can provide low-cost, quick-response solutions to performance trade-offs involving hardware and software modifications.

5. Support of development of future versions of the fire control system (FCS) by characterizing workloads and utilization levels so that future designs can concentrate on resources necessary to optimize performance-pacing tasks.

DESCRIPTION OF THE BASIC SYSTEM

VEST consists of two main portions: (1) an online portion which instruments, collects, and records performance data about TRIDENT Fire Control System activity and (2) an offline portion which reduces and analyzes this data and generates reports. The online portion of VEST includes special purpose hardware for acquiring and processing signals which reflect system activity and the Data Collection Software (DCS) for accumulating and recording such results on magnetic tape. The hardware (Figure 2) includes a specially made Event Trace Unit (ETU) and an off-the-shelf Commercial Monitor (CM). The offline portion of VEST is the Data Reduction Software (DRS) and associated utility programs which run on NSWC's CDC 6700 computer system and process tapes produced by the online portion.

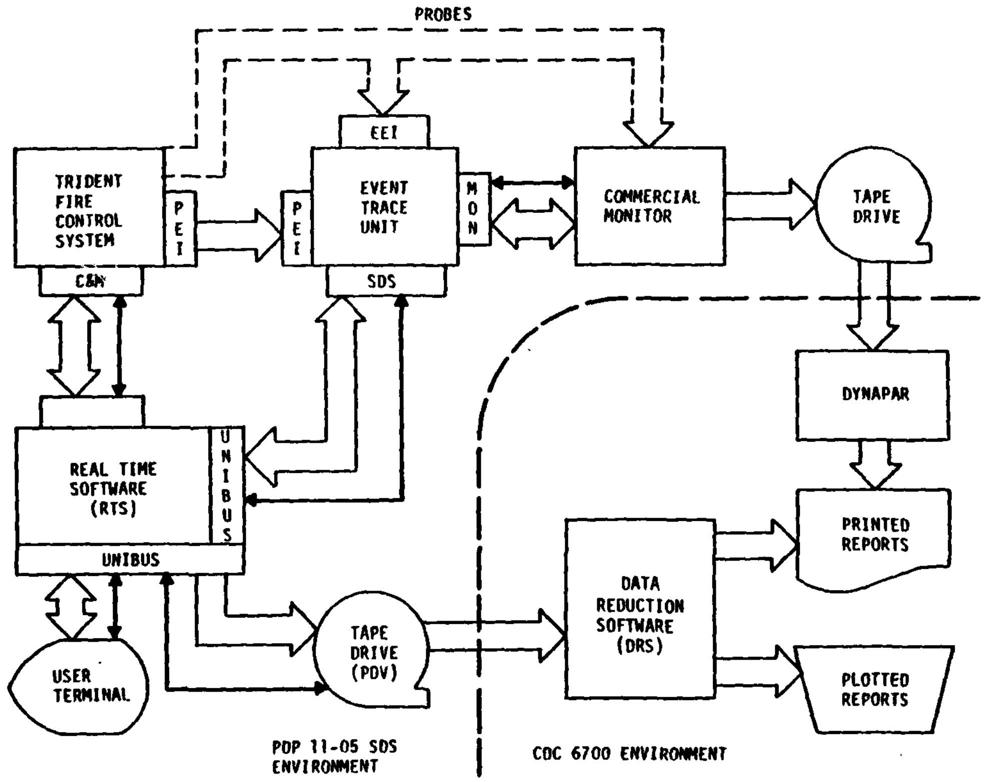


Figure 2. The VEST System

The ETU shown in the center of Figure 2 is a microprocessor-controlled device, the detailed design and implementation of which was done by NSWC from a preliminary Hughes Aircraft Company design. It interfaces with the Performance Evaluation Interface (PEI) of the DCC and can capture data at CPU clock speed. Probe data of discrete electrical events from other parts of the computer group and FCS are available to it and also to the CM.

The performance data collected by the ETU is sent to the SDS's PDP-11 minicomputer for recording on tape. As indicated in Figure 2, selectable data from the ETU may be passed to the CM and vice versa.

The DRS reduces the measurement data collected by the Software Development System (SDS) in order to generate meaningful reports which characterize FCS

activity. CM tapes are also processed on the central computer by its own DYNAPAR proprietary package.

The ETU has within it an Associative Memory (AM) which allows it to "match" any of its contents with the high-speed data stream from the CPU and CM. These data streams may represent locations of code or data in the CPU or any pattern supplied by the CM. An AM allows simultaneous comparisons within the whole memory bank to be carried out on every desired bit of the word being compared. The equipment signals which memory locations, if any, had a "hit." These AM devices are often referred to as "content addressable" memory (i.e., tell the address in which the content is located). The initialization of each VEST experiment establishes the significance of each AM address.

The ETU can also detect preselected external events sensed by probes. The events are subsequently recognized by the DRS software as significant milestones in the progression through the operational sequence. These come either directly from fire control or via the CM programmable logic patchboard. Patchboard features on the CM include logic elements such as AND, OR, NOT, latches, flip-flops, fanout units, decoders and the like. The CM is in itself a powerful measurement device which is preferred for certain instruction mix, CPU throughput and other studies.

An important capability of the ETU is tracing software activity to an extent which was not possible with previous equipment. It allows tracking software tasks, modules, and CPU state changes. Monitoring the activity of certain Launch mode programs or differentiating between the Monitor and the Executive, or just simply limiting the data collected to one portion of the software, are just a few of the things now possible. VEST can also trace program branches and procedure invocations and thereby verify program coverage and correct sequencing. This also facilitates problem area investigation.

The CM is important for PEI as well as non-PEI signals and provides patchboard logic and additional data recording modes. It is needed for accumulating high-speed mappings (distributions) for such things as instruction mix and CPU

throughput studies. Also, it can be used in conjunction with the ETU for Input/Output (I/O) contention and I/O utilization measurements. In instruction mix runs, it would use PEI data passed to it by the ETU. As mentioned earlier, a major feature of the CM is its ability to logically combine signals via the various logic elements contained on its patchboard.

From the user terminal, the ETU is initialized to collect the desired parameters from the FCS. The specification for collection can be quite sophisticated, including calling out raw PEI data, software category change events (that is, changes in CPU state, task, and module), execution of, or reference to, specific program locations, procedure trace, branch trace, and the like. Initial conditions or "set-ups" can be stored, or "canned," and reused whenever desired. With the operator's ability to override or add to certain portions of the canned procedures, the system is convenient yet flexible. Selected printouts of collected data is also an option.

ECONOMY IN DATA REDUCTION

This automated system will greatly reduce the expense of engineering and data-technician work on reducing the data from the measurement runs. In addition, the DRS of the system performs an "analysis" of the reduced data and presents it in graphical and tabular form for easy viewing and comprehension. This is covered in more detail in the next section. Further economies are realized "up front" in the data acquisition phase. The measurement hardware, which is under program control, can be made to collect only certain qualified events and thus greatly reduce the amount of data that the remainder of the system has to handle. Furthermore, there are provisions to permit the user to predefine multiple starts and stops of data collection based on specific portions of the FC operational sequence.

The DRS has the capability of processing the collected data using processing variables (i.e., counters, timers, mappers) and producing various statistics on them, such as the maximum, minimum, mean and standard deviation. These results can then be produced in standardized or user-defined formats.

CLEAR AND EASILY UNDERSTOOD REPORTS

This system supplies reports which are clear and easily understood. The output, in most cases, does not require additional engineering hours in order to gain useful information from the output statistics. VEST provides for selection of a large number of different graphical and tabular presentations. One example (see Figure 3) is a Pie Chart rendition of software utilization results.

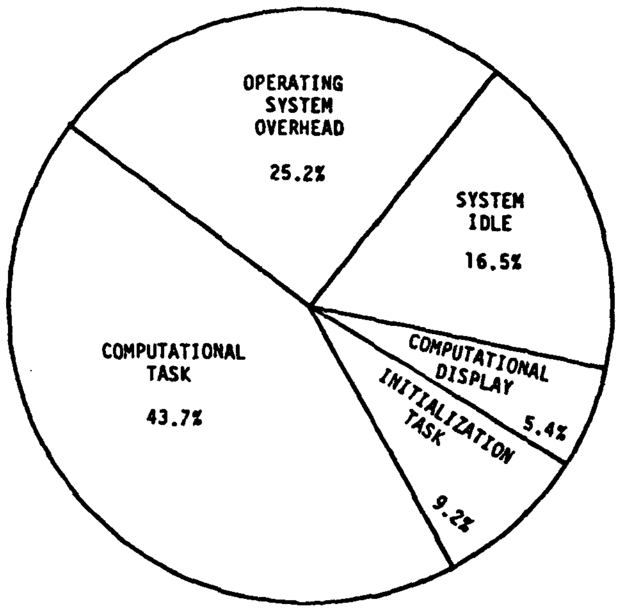


Figure 3. Software Utilization Report (Pie Chart Format)

There are also the Time Line Plots, which are particularly useful in depicting FCS activity (see Figure 4), and the familiar Gantt Chart (bar graph) form which is particularly good for showing periods of activity of different hardware and software components. There are other formats, such as the histogram (see Figure 5) for showing distribution of activity, Kiviatgraphs, Event Listing, Statistical Summary, Exception, and Profile reports. The user may, through these options and report generator facilities, build any report format desired.

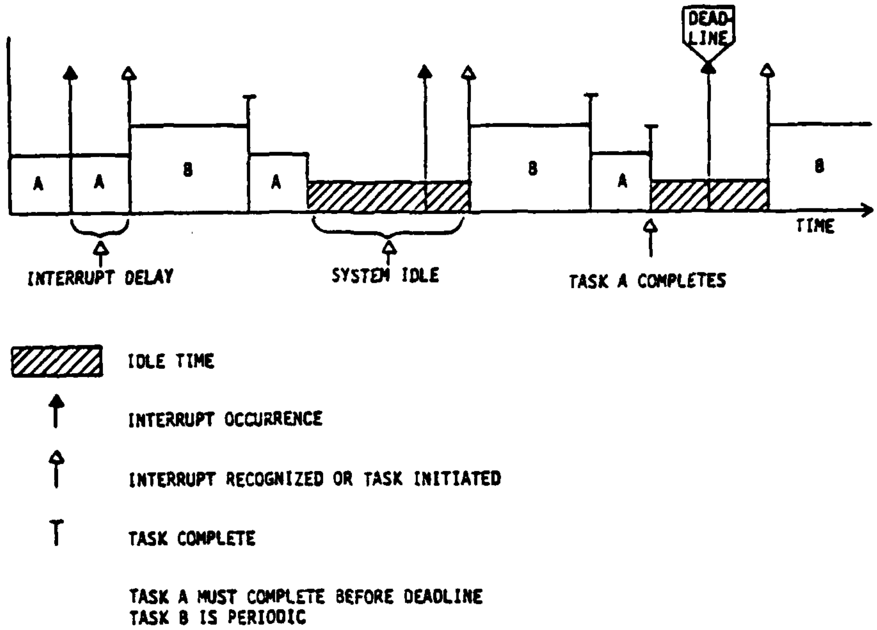


Figure 4. System Line Report (Time Plot Format)

DATE/TIME MODE FILE

\- - - - - -

COMMENTS

START	STOP	VALUE	OPERATING SYSTEM OVERHEAD: 0 20 40 ... 100
0:00	0:10	25.0	X————X
0:10	0:20	10.6	X——X
0:20	0:30	40.7	X——————X
.	.	.	
.	.	.	
.	.	.	

Figure 5. Software Utilization Report (Histogram Format)

REDUCING SET-UP TIME AND ENCOURAGING USE

Verification and Validation (V&V) and Performance Evaluation are both activities high in engineering labor cost for set-up and test design. Not too much can be done about the design time, but much of the set-up effort, with such time-consuming activity as identification of absolute code addresses and other preparatory operations typical of older systems, has been circumvented in VEST. A convenient user interface with a specially designed high-level language is provided, and the ability to select symbolic addresses and events greatly facilitates set-up. In addition, libraries of "canned," often used experimental set-ups and report definitions can be called up to automatically initialize the system in the data collection and data reduction phases. These features should not only save money, but, by making the task easier, thereby encourage a higher level of usage of the VEST system.

CONCLUSION

VEST represents a structured approach to obtain more accurate and revealing data from embedded computer systems. This is not only to establish the performance of existing systems, but to gain more insight into the problem and assist in new designs. The equipment currently in place represents new advances in the ability to monitor and analyze computer system and weapon system activity.

AVAILABLE VEST DOCUMENTATION

1. W. L. McCoy, *TRIDENT Verification and Evaluation System (VEST): Software Requirements Specification*, NSWC TR-3889, Dahlgren, VA, November 1978.

2. W. L. McCoy and D. Carter, *TRIDENT Verification and Evaluation System (VEST): Development Specification*, NSWC/DL TR-3913, Dahlgren, VA, March 1979.

3. T. Owen and A. Dean, *Verification and Evaluation System for TRIDENT (VEST): VEST Support Software Description and Procedures*, NSWC TN 79-280, Dahlgren, VA, November 1979.

4. A. Dean and R. Pond, *Verification and Evaluation System for TRIDENT (VEST): Test Specification and Description*, NSWC TN 79-286, Dahlgren, VA (in preparation).

5. A. Dean, J. Sanchez, R. Pond, and E. Stemple, *Verification and Evaluation System for TRIDENT (VEST): Hardware Description*, NSWC TN 79-288, Dahlgren, VA (in preparation).

6. T. Owen, *Verification and Evaluation System for TRIDENT (VEST): Symbolically Prompted Interactive Test System (SPITS)*, NSWC TN 79-320, Dahlgren, VA, November 1979.

7. R. Pond, A. Dean, and M. McMahan, *Verification and Evaluation System for TRIDENT (VEST): Software Development System/General Purpose Controller Protocol for Initialization and Control of Event Trace Unit*, NSWC TN 79-322, Dahlgren, VA, November 1979.

8. D. Carter and D. Luther, *Verification and Evaluation System for TRIDENT (VEST): Probe Point Library*, NSWC TN 79-334, Dahlgren, VA, November 1979.

9. S. Hankerson, *Data Reduction Software User's Guide*, Dahlgren, VA (in preparation).

10. N. Raines, *Real Time Software User's Guide*, NSWC TR 79-362, Dahlgren, VA (in preparation).

DISTRIBUTION

Defense Technical Information Center Cameron Station Alexandria, VA 22314	(12)
Library of Congress Washington, DC 20540 ATTN: Gift and Exchange Division	(4)
GIDEP Operations Office Corona, CA 91720	
Strategic Systems Project Office Department of the Navy Washington, DC 20376 ATTN: SP2311 SP23112 SP23115	(3)

<u>Local</u>

K50 - Staff	(3)
K51	(2)
K53	(2)
K54	(20)
K55	(2)
K56	(5)
K50-GE	(2)
K50-EG&G	(2)
K60	
K61	(5)
K70	
K74	(2)
X210	(6)
X211	(2)
E41	